

ModelSim 6.6 Series Product Comparison			
Feature	ModelSim PE	ModelSim DE	ModelSim SE
	<i>Block/Small System Simulation, Windows</i>	<i>Quality Critical Designs, Windows/Linux</i>	<i>Large Block/System Simulation, All Platforms</i>
General			
Licensing - Floating License	Option	Option	■
Language Neutral License			Option
ASIC Sign-Off			■
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility			■
Languages			
VHDL 1987, 1993, 2008 (partial)	■	■	■
Verilog 2001, 2005	■	■	■
VHDL/Verilog Mixed Language	Option	Option	Option
SystemVerilog Design	■	■	■
SystemVerilog and PSL IEEE 1850 Assertions		■	
Verilog PLI/VP1	■	■	■
SystemVerilog Direct Programming Interface	■	■	■
VHDL FLI			■
SystemC 2.2	Option	Option	Option
Analog/Mixed Signal (Questa ADMS Product)			Option
Debug			
Interactive Debug	■	■	■
Post-Simulation Debug			■
Enhanced Dataflow Window	Option	■	■
Source Annotation	Option ¹	■	■
Hyperlinked Navigation	■	■	■
Assertion Thread Viewer		■	
Advanced FSM Debug			■
C Debugger	Option ²	Option ²	■
Memory Window	■	■	■
Extra Standalone Viewer	Option	Option	Option
Multiple Waveform Windows			■
Waveform Compare	Option	■	■
Transaction Viewing (SystemC)	Option ²	Option ²	Option ²
JobSpy			■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)			■
Cross Referencing between Windows	■	■	■
Coverage			
Code Coverage (with Toggle Coverage)	Option	■	■
Unified Coverage DataBase (UCDB)	■ ⁴	■	■
Coverage Viewer	■ ⁴	■	■
Test Ranking	■ ⁴	■	■
HTML Reporting	■ ⁴	■	■
Simulation			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations			■
VHDL RTL & VITAL Performance Optimizations			■
Simulation & compile flow optimizations			■
Performance and Memory Profiler	Option	Option	■
Waveform Dataset Management	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)			■
Interactive Simulation	■	■	■
Checkpoint & Restore			■
VHDL 2008 Encryption	■	■	■
Verilog 2005 Encryption	■	■	■
SecureIP	Option ³	■	■
SWIFT Interface / SmartModels	Option	Option	■
Synopsys Hardware Modeler Support			■
Platform Support			
32-Bit OS Support	Windows XP/Vista	Windows XP/Vista/Linux	Linux, Solaris, Windows XP/Vista
64-Bit OS Support			Linux x86-64, Solaris 64

1 - Included in Enhanced Dataflow Option

2 - Included in SystemC Option

3 - Option for use with VHDL

4 - Data generated with code coverage option