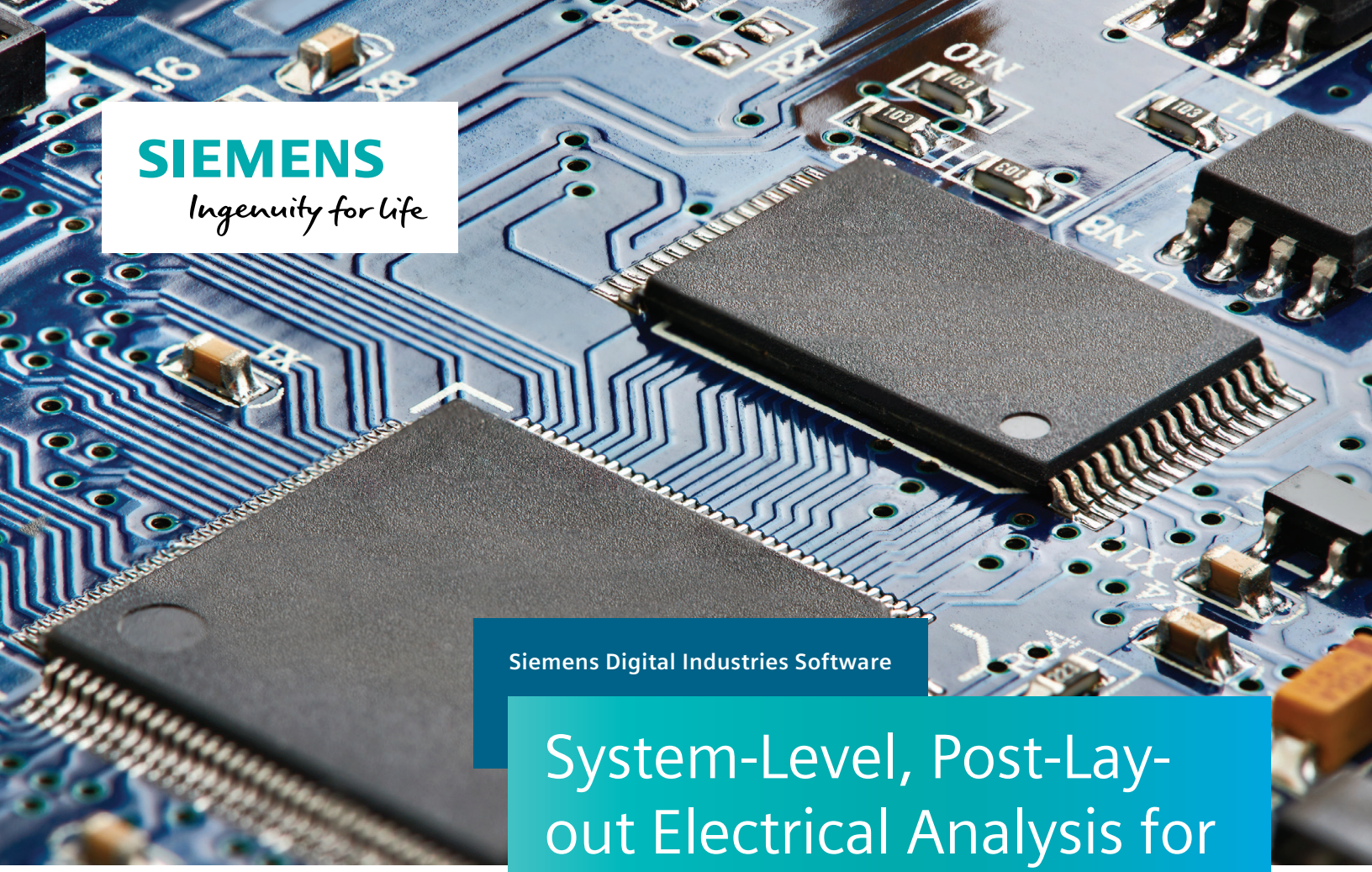

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System-Level, Post-Layout Electrical Analysis for High-Density Advanced Packaging

Executive summary

As HDAP designs become more popular, the need for post-layout simulation (analog) and post-layout STA (digital) flows to augment basic physical verification (DRC and LVS) is growing. Siemens EDA provides an accurate, automated flow that generates the required HDAP netlist for simulation/STA to enable HDAP designers to ensure that the HDAP will perform as designed.

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Introduction

High-density advanced packaging (HDAP) continues to be the promising "More" in the "More than Moore" approach for improved form factor, functionality, and integration of multiple dies built using different technology nodes. Figure 1 shows two examples of HDAP technologies – a 2.5D-IC stacked package with interposers, and a fan-out wafer-level package (FOWLP).

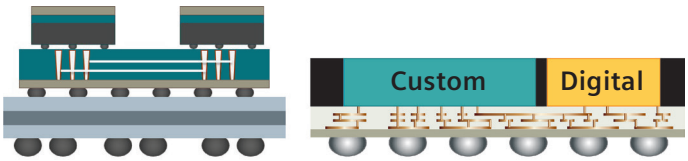

Figure 1: Common HDAP technologies.

HDAP offerings from outsourced assembly and test (OSAT) companies and foundries are continuously increasing. However, the full commercial productization of such offerings will require the assurance of both an acceptable yield and correct (as intended) functionality. This assurance, like that for integrated circuits (ICs), will come from the availability of proven and qualified electronic design automation (EDA) tools and flows that can be used by the design houses to build HDAPs with the confidence that they are compliant with the foundry/OSAT requirements and recommendations.

The need for and general concept of assembly design kits (ADKs) that provide proven, qualified flows for HDAPs has been previously discussed[1,2,3,4]. In addition, there have been analyses of the need for assembly-level layout vs. schematic (LVS) verification for HDAPs[5]. Best practices for an assembly-level LVS process have been proposed, including the required inputs (data, formats, etc.), and likely hurdles and potential errors have been highlighted[6]. There has even been discussion of how parasitic extraction (PEX) could be achieved for packages[7].

However, as HDAP technologies and flows mature, system-level designers want to know if package design rule checking (DRC), assembly-level LVS, and layout vs. layout (LVL) verification (die-to-package alignment, scaling, orientation, etc.) are sufficient to guarantee correct functionality and successful manufacturing of the HDAP. While this question may depend on how complicated the HDAP is, in general, the answer (for now) is no. As HDAP technologies become more and more similar to IC technologies, it is clear that, although the physical verification steps for HDAP may be considered good progress, they are only part of a much more comprehensive flow, one that must account for a more in-depth, system-level electrical analysis. Of course, at the same time, expanded EDA tool support is required to ensure fast, accurate, automated flows that ensure package designers can meet their market schedules and expectations.

HDAP post-layout electrical analysis

In the case of an HDAP design, the foundry/OSAT expects that each component is designed and validated to meet the required HDAP constraints and specifications. For an analog-based flow, the designer must simulate the HDAP system circuitry, including parasitics, to ensure it meets the intended performance specifications. For a digital-based flow, the designer must run static timing analysis (STA) on the complete HDAP system, including parasitics, to ensure it meets the overall system timing budget.

From an EDA perspective, building an automated flow to support these checks/analyses provides assurance that these processes can occur in a consistent, repeatable manner while ensuring accuracy and minimizing runtime. In general, EDA approaches take one of two paths.

Single cockpit

In the cockpit approach, an EDA supplier builds a single simulator infrastructure to support HDAP circuit simulation, parasitic extraction (PEX), and static timing analysis (STA). Although a single interface seems convenient, it forces the designer to use the same design tool for all components at all levels (die and package). This approach may be too restrictive, given that HDAP design and verification typically require the involvement of multiple groups with varying backgrounds and tool preferences.

Although this approach would be useful when building "fully live" heterogeneous HDAPs (i.e., both die and package are under development simultaneously, and can both be edited for performance), this is rarely the case. More commonly, known good dies (which have already been taped out) are used to build an HDAP.

Tool-agnostic

In the tool-agnostic approach, an EDA supplier enables the user to construct the needed system-level connectivity of the HDAP (including parasitics), regardless of which design tools are used to build any one die or the package. Once the system-level connectivity is available, it can be exported in the required format to any circuit simulation/STA tool to simulate or analyze the entire HDAP system. This approach introduces minimum disruption to existing tools/methodologies used for die and package design.

This paper discusses the implementation of a system-level parasitic netlist process for the HDAP using the tool-agnostic approach.

System-level post-layout analysis

To conduct post-layout circuit simulation (analog/RF) or STA (digital) for an HDAP, a system-level layout netlist that accounts for the overall system parasitics must be generated.

To demonstrate the process, we'll explore a digital-based flow example. Before performing this step, the HDAP must be verified for connectivity (LVS-clean). The layout netlist must include a number of components, as described below.

System-level connectivity

For the HDAP as a system, a system-level source netlist in the format required by STA tools (typically Verilog) must be available. This netlist is generated using system-level connectivity planning tools, and is analogous to a schematic in the IC world. Like an IC schematic, this netlist is an "ideal" netlist from a parasitics perspective (i.e., die-to-die and die-to-package connections are assumed to be ideal wires).

Die-level layout parasitics

A parasitic layout netlist must be available for each die in the HDAP. Because these dies have already been verified (taped out) by the IC design teams, these netlists should already be generated in the required format by a well-established IC PEX tool.

Package-level layout parasitics

A parasitic layout netlist must be generated for the HDAP using a well-established, package-level PEX tool. If the HDAP is using an interposer-based (2.5D or 3D-IC) design, then the interposer layout netlist with parasitics can be extracted using an IC PEX tool (because the interposer manufacturing process is similar to the die back-end manufacturing process).

Die/package interface parasitics

A flow that can extract the coupling capacitance between the die and the package in an HDAP (usually called the die/package interface) is required to account for unintended electrical interactions (parasitics) between the die and the package in the HDAP.

Pre-processing

To ensure accuracy in the results, this flow must consider two questions about the HDAP design before generating the interface RC model and running the parasitic extraction process.

Is interface extraction required?
Based on the specific HDAP technology, accounting for such interactions can range from "required" to "not necessary." For example, in FOWLP technologies, the die and the package are usually stacked with close proximity, which suggests the need to account for any interface coupling. In standard 2.5D stacking approaches (interposer-based), the spacing between the die and the interposer is usually large, so the interface coupling may typically be ignored.

Which layers from each die must be included in the interface?
Assuming that the flow must account for interface coupling, which layers must be included in this interface from each die? The more layers included from each die, the higher the accuracy, but this accuracy comes at the cost of longer run times and more complexity. At a minimum, the interface database must include two physical layers – the bottom-most layer from the top die and the top layer from the bottom die/package. The foundry/OSAT typically provides a recommendation as to which layers to include, allowing the designer to add more layers as needed to verify the accuracy of the results.

Annotated interface database generation

Once the pre-processing questions are answered, an interface database must be generated in the required format (typically GDS), annotated with connectivity information and accounting for the expected (x,y) placement locations, scaling, and orientation. An EDA assembly creation tool can automatically grab the needed layers from each die/package, and generate this interface database with the necessary annotation.

Interface RC model/rules generation

The flow must next generate the required RC rules/models for the interface. Technology data/RC models are delivered by the foundry/OSAT for each separate die and package, as this data is tightly related to how each component is manufactured. However, for the interface, the technology data/RC models must include both the die and the package. The RC model generation process uses the "required layers" information and the technology data supplied for each component to generate the interface RC models based on the interface technology data (vertical description of the layers stack in both the die and the package). The RC model generation process must be flexible, so the designer can add/remove layers and still get accurate results. Just like the annotated interface database, an EDA assembly creation tool can provide an automated and flexible flow to generate the interface technology data and RC models.

Interface parasitic extraction

Once both the annotated interface database and the interface RC models are available, the designer can run an IC-based PEX tool to generate a layout netlist annotated with the interface parasitics. IC-based PEX tools are used instead of package-based tools because typically only the very top layers of the package are selected for the die-to-package interface. In HDAP technologies, the die is mounted directly to those layers, so they are very similar to the top die layers in terms of dimensions and shape. However, designers must be aware of and avoid double counting – some parasitics that are already extracted in the die (or the package) will be re-calculated when extracting the die/package annotated interface.

Once all of these parasitics are extracted, the system-level connectivity data (for example, a Verilog netlist) can call the die-level layout parasitics data, the package-level layout parasitics data and the die/package interface parasitics data to form the needed input for static timing analysis tools. The HDAP designer can run STA and observe the timing results to see how they are affected by the system-level parasitics.

Figure 2 shows a block diagram of the complete die/package interface parasitic flow.

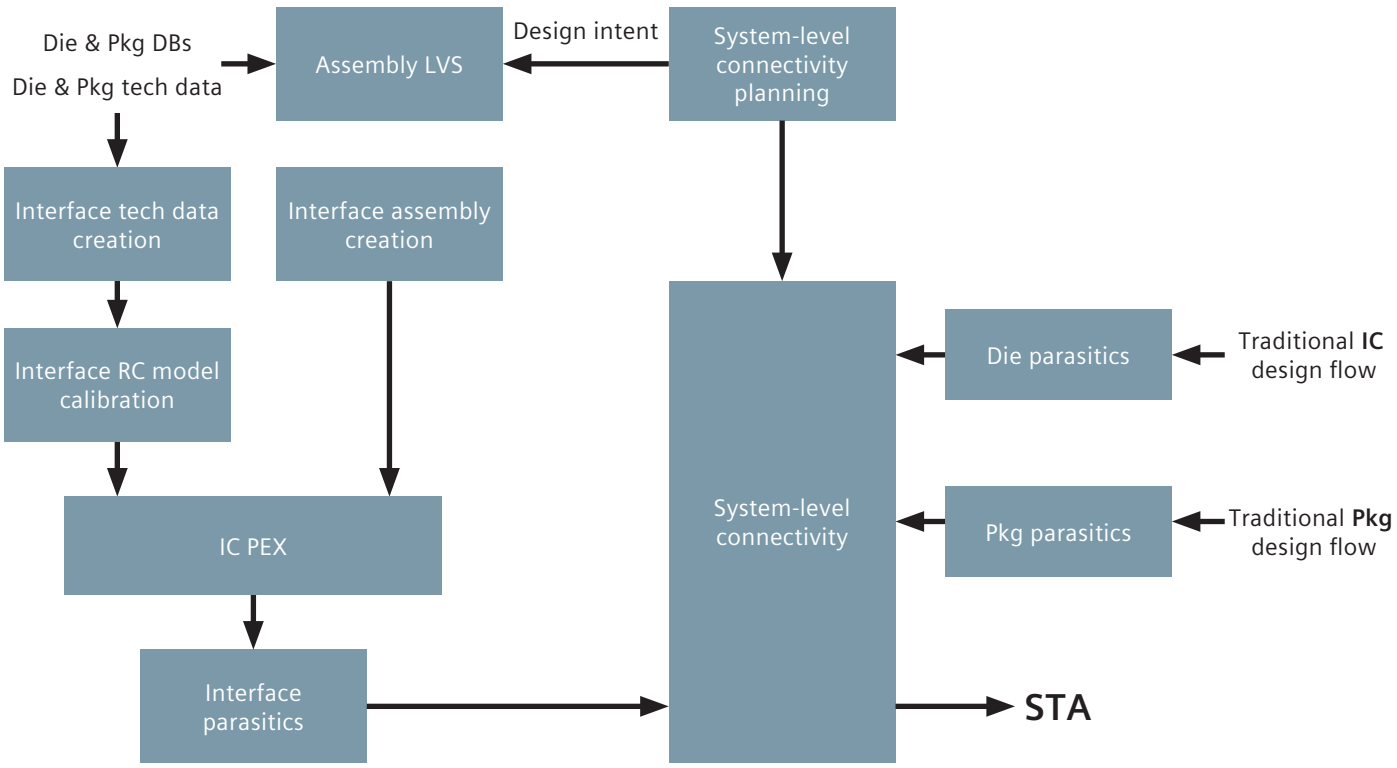

Figure 2: Complete HDAP parasitics flow for digital STA process.

Siemens EDA flow for HDAP post-layout static timing analysis

Siemens EDA, a part of Siemens Digital Industries Software, has a complete automated flow that enables designers to generate the needed netlist for STA, using multiple tools from both IC and packaging disciplines. The Xpedition® Substrate Integrator (xSI) tool performs the HDAP system-level connectivity management and planning. The xSI tool can generate a system-level connectivity information in multiple formats (e.g., a spreadsheet-like netlist for HDAP LVS, or a system-level Verilog netlist for downstream analysis like STA). The Calibre® 3DSTACK tool enables HDAP physical verification (DRC, LVS, and LVL), and generates the required inputs for PEX tools. In the STA flow, the Calibre 3DSTACK tool automates the interface assembly creation (including connectivity annotation), the interface technology data creation, and the interface RC rules/ models calibration as one step (i.e., one Calibre 3DSTACK run). The Calibre xACT™ IC PEX tool can read in the required inputs from the Calibre 3DSTACK tool natively. It also provides options that can be used to prevent double-counting of parasitics. Figure 3 shows the post-layout HDAP analysis flow annotated with Siemens EDA tool use.

This flow has been verified by TSMC for use with the TSMC InFO reference flow, providing InFO designers with confidence that their InFO design will perform as designed and as intended[6].

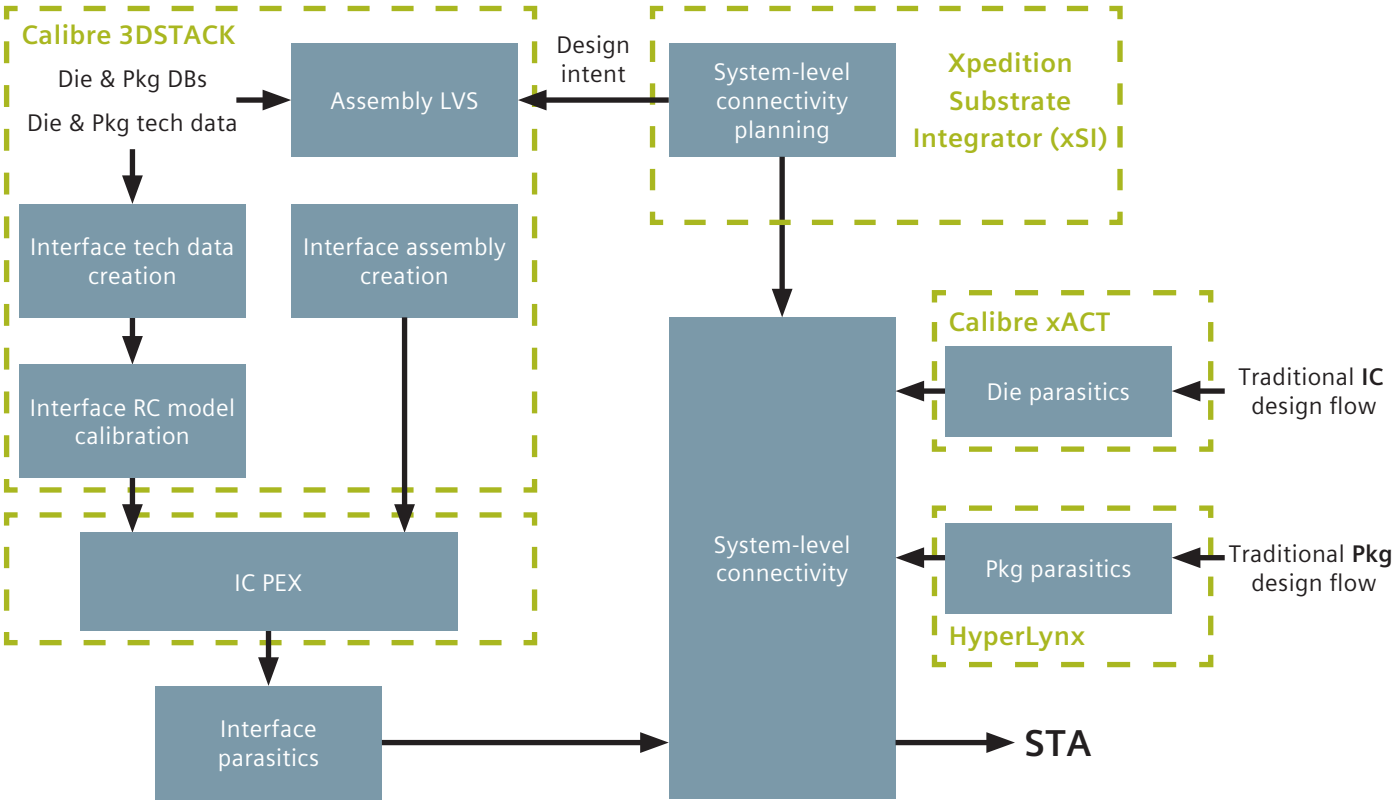

Figure 3: Complete HDAP parasitics flow for digital STA using Siemens automation.

Conclusion

As HDAP approaches become more popular, the need for post-layout simulation (analog) and post-layout STA (digital) flows to augment basic physical verification (DRC and LVS) is apparent. By providing an accurate, automated flow that generates the required HDAP netlist for simulation/STA, EDA companies enable HDAP designers to ensure that the HDAP will perform as designed. Siemens EDA provides a complete, proven flow that generates HDAP system-level connectivity while accounting for die, package, and die/package interface parasitics. Confidence in HDAP manufacturability and performance is essential to their continued growth and market success.

References

1. John Ferguson, Tarek Ramadan. "The future of package design verification: assembly design kits," Siemens Digital Industries Software, October, 2015.
2. Andy Heinig. "Why use an assembly design kit and assembly design flow?," Semiconductor Engineering. February 8, 2018. https://semiengineering.com/why-use-an-assembly-design-kit-and-assembly-design-flow.
3. John Ferguson, Tarek Ramadan. "Assembly design kits are the future of package design verification," 3DInCites. August 3, 2015. https://www.3dincites.com/2015/08/assembly-design-kits-are-the-future-of-package-design-verification.
4. Tarek Ramadan. "Crossing the chasm: bringing SoC and package verification together with Calibre 3DSTACK," Siemens Digital Industries Software. January 2017.
5. Tarek Ramadan. "Package designers need assembly-level LVS for HDAP verification," Siemens Digital Industries Software. December 2017.
6. "Mentor extends solutions for TSMC InFO and CoWoS design flows to help customers continue IC innovations," Press release, Siemens Digital Industries Software. Sept. 13, 2017.
7. John Ferguson, Dusan Petranovic. "Full 3D-IC parasitic extraction," Tech Design Forum. June 8, 2014. http://www.techdesignforums.com/practice/technique/full-3d-ic-parasitic-extraction.

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