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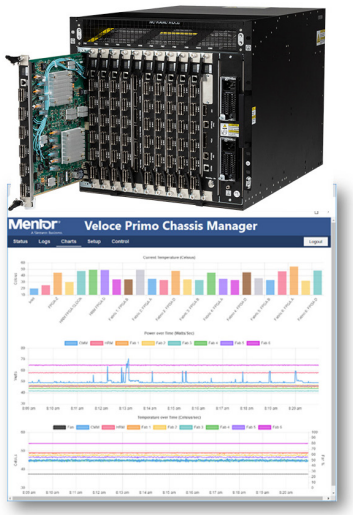
Veloce® Primo™ Enterprise Prototyping Solution

The Veloce® Primo™ enterprise prototyping solution combines scalable capacity and high performance with emulation compatibility delivering quick bring-up required to realize the benefits of early, pre-silicon software enablement and full system validation.



Scalable Enterprise Prototyping Solution

With the ability to scale up to 320 FPGAs, the Veloce Primo enterprise-level prototyping has the capacity for very large SoCs, multi-die and chiplet designs exceeding 10 billion gates. Veloce Primo offers multi-user, single FPGA granularity and supports both virtual and in-circuit emulation (ICE) test environments. As an enterprise prototyping platform, Veloce Primo delivers industry-leading density and cost of ownership for lights-out with up to 80 FPGAs in a standard 42u rack and best-in-class power consumption and total cost of ownership.

Veloce Primo comes standard with remote management and job scheduling capabilities to maximize the accessibility and utilization of prototyping resources. Through an easy-to-use web browser interface, the status of each Veloce Primo system can be monitored and controlled.

Benefits

- High-performance pre-silicon solution for software enablement and system validation
- Veloce Strato compatibility enabling same RTL, same virtual environment
- Scalable across all prototyping use models
- Scalable from a single FPGA to billions of gates
- Enterprise prototyping platform with lights-out management
- Excellent debug productivity for ICE and virtual use models
- Multi-user support with single FPGA granularity
- Rich set of virtual and ICE solutions
- Highest density, lowest power for best TCO

Prototyping Software (Veloce OS): Performance with Quick Design Bring-up

Uniquely, the Veloce OS for Veloce Prototyping Software (VPS) is the only enterprise prototyping software solution combining the performance of prototyping with the benefits of quick design bring-up and turnaround time. While competing solutions force the Hobson's Choice of quick bring-up or fast run-time via different compilation flows, VPS delivers a single prototype compilation flow with a sliding scale of performance optimizations. VPS shares a common RTL front end with Veloce Strato delivering the highest productivity available in an emulation-prototype continuity of hardware-assisted verification.

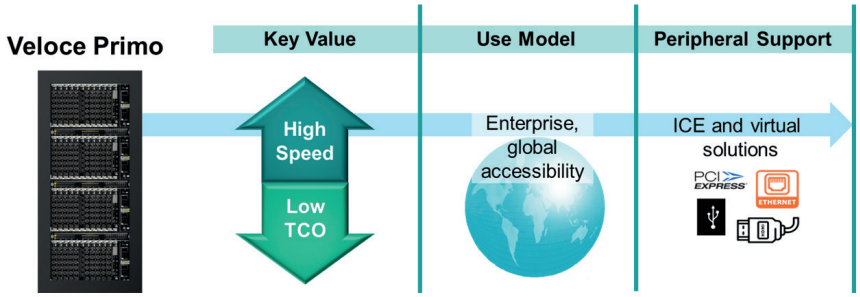
In fact, VPS is the first prototyping solution proven to deliver same design RTL and virtual environment compatibility between emulation and prototyping, maximizing reuse. Eliminating the cost in resources and time to create and maintain separate design models and separate environments. VPS also enables rapid turn-around when rebuilding prototypes from fresh RTL code drops.

VPS automates the conversion of ASIC-targeted designs into an efficient FPGA implementation including complex clocking, while retaining clock ratios, inferred multi-port memories and various styles of latches. Partitioning of the design across multiple FPGAs is timing-driven and efficient in resources with the user in control of resource vs. performance trade-off decisions. Users can direct as much or as little of partitioning as needed to achieve runtime performance objectives. Mapping the design into FPGA resources delivers high quality of results (QoR) enabling single FPGA designs or logic blocks within one FPGA to achieve 100+ MHz performance.

Flexible and Scalable Use Models

Veloce Primo and VPS support the full range of traditional prototype uses spanning large farms running IP blocks to large subsystems, full SoC and multi-die/chiplet SW-driven validation and SW development & test often using ICE interfaces. It also makes an excellent partner to Veloce Strato by enabling more cycles per dollar for many workloads, typically using virtual environments that can effectively be regressed on Veloce Primo.

For the more traditional prototyping use models, a rich set of ICE solutions for a wide variety of protocols enables plug-fest level verification and validation. An impressive library of Soft-model memories can be used with ICE and virtual environments providing backdoor access for loading and dumping memory contents while eliminating the headaches of managing multiple memory hardware configurations. Support for Veloce Transactor Library (VTL) and VirtuaLAB soft environment models make it easy to move workloads between Veloce Strato and Veloce Primo.



TestBench Xpress (TBX) is Veloce's implementation of the SCE-MI2 standard and is the foundation for reusable environment models such as VTL and VirtuaLAB. TBX also enables users to create high-performance software environments and transactors for reuse between emulation and prototyping.

Advanced Debug Capabilities

VPS delivers the industry's best prototype debug capabilities, regardless of the prototype's use model and environment. For ICE environments, VPS delivers broad and deep, probe-based, at-speed debugging. Tens of thousands of signals per clock domain can be instrumented at compile time, with runtime selection of the trace set, conditional capture, trigger conditions, and events. Many seconds of runtime can be captured by streaming trace data to memory or disk without the need for additional hardware set up and configuration. When virtual environments are used, full register visibility, with reconstruction of combinational nodes, is available for maximum debug visibility and productivity. VPS can also export the prototyped design to Veloce Strato for even better debug productivity.

Veloce HW-assisted Verification Platform

Veloce Primo extends the capabilities and verification & validation flow productivity of the Siemens Veloce HW-assisted verification platform.

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83490-rev2_J1 02/21