



A Siemens Business

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# **PADS® Professional Release Highlights**

Software Version PADS Professional VX.2.3

February 2018

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## Introduction

Built for the independent, multi-discipline hardware engineer who does it all, PADS Professional utilizes Xpedition® technology that can handle the most demanding and complex designs, where other solutions fail.

PADS Professional is powerful, but it's also easy to learn, use, and afford. It's designed to give the experienced user all the horsepower they need, yet intuitive, so casual or occasional users can accelerate their time to productivity.

The full flow of PADS Professional enables you to design, validate and manufacture PCB-centric systems incorporating advanced FPGA devices.

## New Products and Features

### New Product Options

- **PADS Professional Rigid-Flex Design** - A new Rigid-Flex PCB design cost option is now available. Full 3D environment for design and validation of complex rigid-flex structures helping you achieve smaller, cheaper, more reliable products.
  - Stack-up regions defined by multiple board outlines to simplify modifications
  - Define unique stack-up types (e.g. embedded or bikini cover lay, stiffeners)
  - Bend areas define where and how the design will bend
  - Flex-aware placement & routing produces high quality results
  - 3D bending and 3D DRC

### Licensing

All licensed options that were previously available only as Node Locked are now also supported with Floating licenses

- Advanced 3D
- RF Design
- New Rigid-Flex Design
- Advanced DRC
- FPGA-PCB

### ECAD/MCAD Collaboration

The MCAD Collaborator is not now available as standard functionality in the core product at no additional cost to the user.

Previously it was included as part of the Advanced 3D option.

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# PADS Professional (DX) Designer

There are several ease of use improvements and new functionality for the VX.2.3 release.

## Assign Reference Designators under user control (IDEA D6577)

New functionality to allow renumbering from the schematic

- Set scope
- Set prefix/suffix
- Set increment
- Set direction
- Run pre-check – Do not modify components

## Display Control

Enhancements to new display control introduced in VX.2.2

- Options expanded and re-organized
  - Pin Type Arrows
  - Ripper Index
  - Rulers
  - Notes
- Show Pin Type Arrows for hierarchical blocks only
  - Idea - D15026
- Slider Control for 'Selection Highlight'
  - Idea 15802
- Support ~ in name
  - Idea D12887
  - Option to use ^ as over-bar character instead of ~
- Cross-probing
  - Zoom to fit
  - Zoom to pin
  - Zoom level control

## Part Replace

Improvements to pin mapping dialog:

- Enhancements following VX.2 Beta & VX.2.1 feedback
- Improved user visualization
- Support for multiple symbols

Improvements to property mapping dialog:

- User choice of mapping overrides is saved

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- Library only
  - Schematic wins
  - Library wins
  - Mapping scheme is used on next invocation

## Miscellaneous Enhancements

- Improved configuration of Search
  - Column chooser
  - Hide 'Group' bar
  - Prevent selection of unsupported data sources
  - Selection boxes (Excel like) in filters
  - Settings to follow corporate WDIR
    - Settings moved to DxDesigner.xml file
- Support 'Dashed' lines for unplaced parts in Variant Manager

## IDEAS

The following additional IDEAS have also been addressed:

- D2668 - Dxf in or Pastespecial in symbol editor for logo support
- D7256 - Highlight net through whole schematic
- D10985 – Double click to open down on functional blocks in DxD
- D11928 - New way to display 4-way intersection of nets
- D12692 - "Click to Edit" should not reset zoom or remove selection
- 3980 - = "Fit All"command All Placed Symbols Should Be Shown Just As "Fit Selected" Does
- 14427 – Out of Grid item move
- 15706 - Verify results should include Ref Des

## HyperLynx SI/PI/Thermal VX.2.3 - Overview

HyperLynx SI/PI/Thermal VX.2.3 is the follow-on release to HyperLynx 9.4.2, and now uses the same release numbering scheme as our other HyperLynx products and as our PCB Layout Design flows (Xpedition & PADS). This release contains a number of new features, as well as incremental improvements which are extremely helpful for both SI and PI analysis. Many of the features are targeted towards more efficient analysis and design of multi-Gbps SERDES channels, but with continued improvements to analyzing sub-GHz interfaces as well. The following new features are available in this release:

### **SERDES Wizard**

One of the biggest features in the HyperLynx VX.2.3 release is the first version of the SERDES Wizard. This new Wizard makes the process of analyzing serial interfaces much more streamlined, allowing for analysis of every signal on a bus all at once. In this first instantiation of the Wizard, it will support S-parameter extraction and analysis, including advanced metrics such as Insertion Loss

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Deviation and Power Sum Crosstalk. It will also support Channel Operating Margin (COM) as well as some protocol-specific verification modules for busses like USB and PCI Express. Other checks include simulation-based skew and impedance checks, to ensure maximum margins.

The Wizard can be run in a variety of modes. In Compliance-only mode, the Wizard runs only the analysis types required to ensure compliance for a specific protocol. The Wizard will also run on S-parameters taken from measurements, whether they be a single large S-parameter or a group of coupled 4-port S-parameters. The full SERDES Wizard allows users to choose from all available analysis types to cater a solution to their preference.

## **Automatic 3D Area Creation**

Another feature that allows for huge efficiency gains in analyzing multi-Gbps SERDES channels is the automatic 3D area creation. As frequencies increase, certain areas on the board such as vias, DC blocking capacitors, and chip breakouts require a full 3-dimensional electromagnetic solver to be properly characterized. In HyperLynx VX.2.3, all of those areas can be automatically identified, solved, and replaced with solved models for simulation.

In previous releases, the 3D pattern-matching has been available to find areas of the board that match other areas, so that a single solved model can be used for all. This made a drastic improvement in the efficiency of using the 3D solver and made large-scale 3D modeling truly practical. Now, in HyperLynx VX.2.3, users can find all the 3D areas automatically, including all the matching areas, and send off those areas to be solved using the HyperLynx 3D solver. The automatic 3D area creation has been in Beta for a couple years and is now getting officially released in HyperLynx VX.2.3.

## **General Batch Wizard**

In previous HyperLynx versions, users could perform batch simulation of signals using the General Batch Wizard and/or the Advanced Batch Wizard. In VX.2.3, the capabilities of those two Batch Wizards have been combined in the General Batch Wizard, which also features a number of improvements for more efficient Batch simulation. In the General Batch Wizard, users can select from traditional SI analysis types like Signal Quality, Delay, and Crosstalk, as well as Quick Analysis options and EMC analysis. Signals can be grouped into net groups for more efficient application of constraints and analysis. Once the batch analysis completes, results are generated using the traditional text files and spreadsheets, as well as the more modern, easily-navigable HTML reports.

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## Support for Hatched Planes in LineSim

In HyperLynx VX.2.3, the transmission line models in LineSim have been enhanced to support hatched planes. This includes the integration of a new specialized hatched plane solver. Two new transmission line types have been added with hatched plane references: one for microstrip and another for stripline. Additionally, the coupled transmission line capabilities have been enhanced with a new reference conductor type for hatched reference planes. All the new transmission lines allow the user to specify the hatching parameters like width and pitch, as well as the orientation of the trace to the hatching.

## Improved Loss Modeling in Traces

To allow for greater accuracy at high frequencies, the loss modeling in the transmission line models in HyperLynx has been improved. This includes the addition of supporting new types of surface roughness models, including Modified Hammerstad and Cannonball roughness models.

## DC Drop Visualization Improvements

Via currents have been added to the plots generated by DC Drop analysis. Users can now view 2D/3D plots of the via currents to more quickly pinpoint areas of excessive via current. Furthermore, the current vector plots have been enhanced to be more intuitive, showing current vectors as arrows of varying color and size to depict the flow of current.

## Other DC Drop Analysis Enhancements

Models created for DC Drop analysis can now be saved and re-used for multiple versions of a design, or across multiple designs. The models can be saved as .hlpimodel files, and assigned by .ref or .qpl files.

Also, the voltage constraint for DC Drop will now default to being a percentage instead of a fixed voltage. This allows for quicker application of a single percentage for multiple voltage nets for batch analysis, as well as the more intuitive representation of the constraint as a percentage.

## Fast-Settling Capacitor Model

A common issue with simulation of multi-Gbps SERDES interfaces is the settling time of capacitor models. There are a number of documented workarounds to this issue on Support Center. In HyperLynx VX.2.3, users no longer need to employ these workarounds, as a built-in fast-settling capacitor model has been added. This model works by the simulator generating two DC operating points prior to simulation, which allows for rapid calculation of the capacitor bias voltage, and avoidance of the lengthy time for the capacitor to “settle”. This model is disabled by default, but can be toggled under the Advanced Options tab.

## Package Wrapping Utility

A new utility has been added to allow for easily adding a package model to an IBIS model. Due to limitations in the built-in IBIS package model, vendors often provide models for their packages in S-

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parameter and SPICE format. The new wrapping utility provides an intuitive GUI for mapping the package model nodes to pins in the IBIS model, with a choice of formats.

## **Touchstone Viewer Improvements**

In the Touchstone Viewer, users can now save their settings as a project to be re-used later. Also, various viewing improvements were made, including on-the-fly mode conversion for looking at the mixed-mode version of an S-parameter.

## **Total Net Capacitance**

In addition to being available in the General Batch Wizard, the Total Net Capacitance for a net can be quickly seen by right-clicking on the net and viewing the Net Statistics. The capacitance is reported as a total net capacitance, which includes the loading from any attached IC models, and the capacitance of just the trace metal itself.

## **Automation and Scripting**

A scripting infrastructure has been built into HyperLynx for the past several releases, and in this release a scripting debugger has been added to make it much easier to debug scripts. There are also a number of script tutorials available in the HypFiles folder in the install directory.

# **Valor NPI**

The following new features are available in this release.

### **MRA Revolution**

- Additional fabrication checks in ADM
- Analysis precondition for Rigid Flex/Flex, HDI and Microvia
- Analysis Configuration Manager
- Analysis results link to defined constraint
- Classification evaluation within ADM
- Classification of constraints by features/nets attributes
- ADM compatibility to Valor NPI version
- ADM Classification Set templates

### **Panel Designer**

- Panel Designer assistant
- Automatic Assembly Design with variable panel sizes
- Break tabs with component avoidance



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## Analysis

- Support of area classification results by layers in HDI and Microvia

## CAM Compare

- Sharelist integration (IDEA D11102)

# Authorization Codes

To use the latest releases, you must be on support contracts for these products as of February 2018. For more information about "Exact Access" authorization code formats, see the explanation on Support Center at [Exact Access Licensing](#)

You may download your site's existing authorization codes from Support Center at [Account Center Licenses by site](#)

# Supported Platforms

## Overall Notes

- Specified patches below are minimum levels. Later versions of the patches are valid, supported configurations.
- Except as noted, all products are supported on all platforms.
- Processor and Memory requirements vary based on the mix of applications being used, the design complexity, and infrastructure requirements. Individual needs may vary from those published below.

## Processor Note for Intel/AMD Processors

All Windows variants run on Intel or AMD x86 or x64 processors. In the past, the processor GHz speed determined the performance, but recent changes in the internal architecture of both Intel and AMD processors have made these comparisons difficult. Therefore, the following recommendations are being made for **all** Windows systems.

- Supported processors and systems are those manufactured since 2006 which conform to the subsequent requirements.
- Intel Celeron processors are not recommended.
- Minimum requirement is a dual-core (or dual processor) system. A quad core is recommended for improved overall system performance. A hyperthreaded processor should be considered a single processor, not a dual processor.
- For best results, maximize processor speed and L1/L2/L3 processor cache memory.

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- Typically, cost is the best indicator of performance, and extra investment in processor capability returns better system performance.

## Microsoft Windows 7

Microsoft Windows 7 (32 and 64 bit versions), Professional Edition, Ultimate Edition, and Enterprise Edition are supported.

While there is no known issue with running Microsoft Windows 7 Starter Edition and Microsoft Windows 7 Home Premium Edition, the product has not been tested with these editions, and therefore is not supported.

**Kernel Configuration:** N/A

**Processor:** Dual-core Intel or AMD processor minimum. See [Processor Note for Intel/AMD Processors](#) above.

**Memory:** 8GB recommended.

**Swap Space:** 2x the amount of RAM.

## Microsoft Windows 8.1

Microsoft Windows 8.1 Professional Edition, Ultimate Edition, and Enterprise Edition are supported.

**Kernel Configuration:** N/A

**Processor:** Dual-core Intel or AMD processor minimum. See [Processor Note for Intel/AMD Processors](#) above.

**Memory:** 8GB recommended.

**Swap Space:** 2x the amount of RAM

## Microsoft Windows 10

Microsoft Windows 10 (32 and 64 bit versions), Enterprise Edition and Pro Edition are supported.

While there is no known issue with running Microsoft Windows 10.0 Home Edition or Educational Edition, the product has not been tested with these editions, and therefore is not supported.

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**Warning:** The new Microsoft Edge Browser delivered with Windows 10 is not supported with PADS Pro VX.1.2 and Later.

**Kernel Configuration:** N/A

**Processor:** Dual-core Intel or AMD processor minimum. See [Processor Note for Intel/AMD Processors](#) above.

**Memory:** 4GB Minimum, 8GB recommended

**Swap Space:** 2x the amount of RAM